

### **DAT 6000 SERIES**

# ANALOG to DIGITAL INTERFACE UNITS for PLC DATA ACQUISITION

- USER MANUAL -



### **FEATURES**

- Analog Signal Acquisition on PLC digital I/O
- Models and analog inputs : DAT6023 - 4 channels for V or mA
- 16-bits resolution with high F.S. accuracy
- Linearization function for Tc and RTD
- PC and DIP-SWITCH configurable
- 3-ways 2000Vac galvanic isolation
- In compliance with EMC directives CE mark
- 12.5 mm thin profile housing
- DIN rail mounting

### **APPLICATIONS**

- Factory Automation
- Building Automation
- Agricolture Automation
- Chemical Industry Measurement
- Security system
- Machine Control

### Introduction

The DAT6000 series is an evolution in the connection techniques of the analog signals to the PLC.

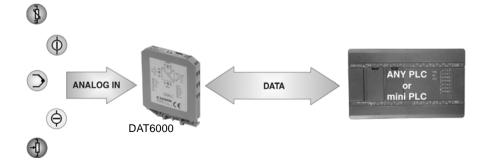
The devices of this serie performs many functions as: amplification, linearization, isolation, filtering and conversion of analog signals, coming from various sensors, in a high resolution digital signal. The digital signal is transferred to the PLC by a bus connected to any one of the controller's digital input. It is composed by a series of 16-bit 'words' containing the values of the analog signals to be measured. The transfer is PLC controlled by a clock signal coming from one of its output ports. At every clock pulse a bit of the data is transmitted.

Using few and simple instructions the PLC is even capable to acquire more analog signal on a single digital input.

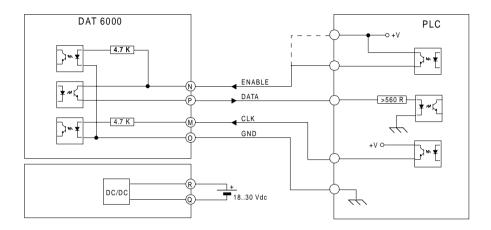
The devices are also provided of an Enable signal which, handled by the controller, allows to "multiplexing "many devices on the same digital input.

The DAT6000 series is composed of the following devices:

Device	Channels	Input Type
DAT 6011	2	mV and Tc
DAT 6012	2	RTD, Res. and Pot.
DAT 6013	2	V and mA
DAT 6021	4	mV and Tc
DAT 6023	4	V or mA



### How to connect DA T6000 to PLC



The serial interface of the DAT 6000 series devices is shown hereup. Input and output signals are optoisolated among analog input and power supply. The DATA signal circuit is powered directly with the ENABLE signal voltage. Without the ENABLE signal, the data output is disabled. The ENABLE input (terminal N) can be connected directly to the supply voltage, leaving available a PLC output port; in this case the data output is always enabled. Using the ENABLE signal, the CLK signal can be always active, because when ENABLE signal is off, the microprocessor ignores the clock signal, stopping the data sending; by this way, it is possible to connect many devices in multidrop connection, using few PLC I/O ports.

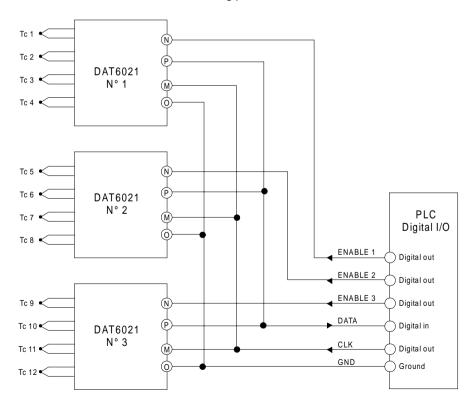
The power supply of the DAT6000 is isolated from the serial interface so that the auxiliary supply of the PLC can be used to power it.

### **Multidrop connection**

The CLK input and the DATA output of the DAT6000 devices are actives only when the ENABLE signal is on. Consequently It is possible to connect all the DATA signals to the same PLC digital input and all the CLK signals to the same PLC digital output. Devices can be activated one by one sending the ENABLE signal to the selected device only.

As shown in the figure below, using n°3 DAT6000 devices it is possible to read the value of up to 12 analog sensors using only 4 PLC digital outputs and 1 PLC digital input. Each new device connected will use only one more PLC digital output (ENABLE).

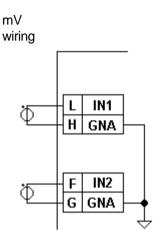
Changing the device type, it is possible to create many combinations of analog inputs (i.e.: 4 Tc inputs on the first device, 4 mA inputs on the second device and 2 Potentiometer inputs on the third device), without to change the wiring to the PLC and the software data reading procedure.

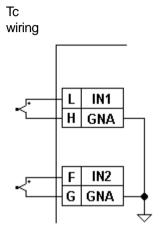




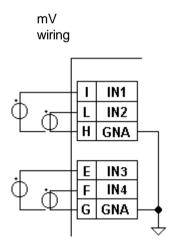
### **Analog Inputs connection**

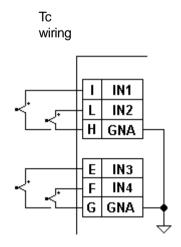
### **DAT 6011**





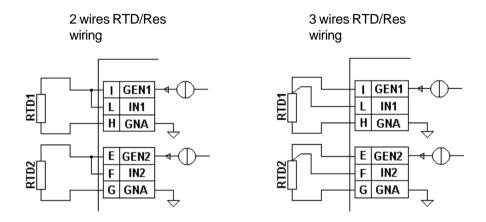
### **DAT 6021**

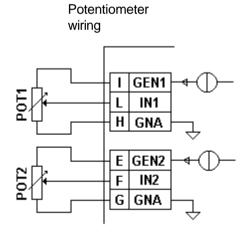




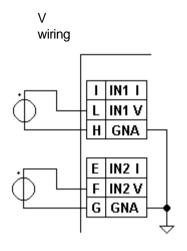


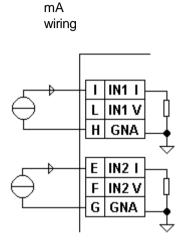
### **DAT 6012**



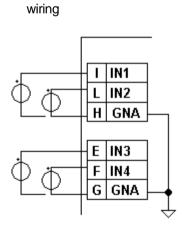


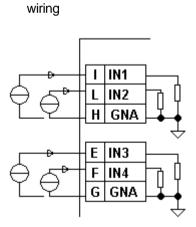
### **DAT 6013**





### **DAT 6023**





mΑ



### **Technical Characteristics**

### **Analog Inputs**

### **DAT 6011, DAT 6021**

mV		
Input	Min	Max
50 mV	-50 mV	+50 mV
100 mV	-100 mV	+100 mV
500 mV	-500 mV	+500 mV
1000 mV	-1000 mV	+1000 mV

Thermocouple			
Input	Min	Max	
TcJ	-210 °C	+1200 °C	
Tc K	-210 °C	+1372 °C	
TcT	-210 °C	+400 °C	
Tc E	-210 °C	+1000 °C	
Tc R	-50 °C	+1767 °C	
Tc S	-50 °C	+1767 °C	
Tc B	+400°C	+1825 °C	
Tc N	-210 °C	+1300 °C	

Channels: 2 ( DAT 6011 )

4 ( DAT 6021 )

Input Type:  $\pm$  50 mV to  $\pm$  1V

Tc: J, K, T, E, R, S, B, N

± 0.1 F.S. Calibration Accuracy:

± 0.2 % for Tc Linearity: < 0.8 uV/Ohm Lead wire resistance influence: Input impedance: > 10 MOhm Cold Junction Compensation: ± 0.5 °C

Thermal Drift: ± 0.005 % F.S. /°C Sampling Rate: 10 samples/sec

Bandwidth: 4 Hz



### **DAT 6012**

RTD			
Input	Min	Max	
Pt100	-200°C	+850°C	
Pt1000	-200°C	+200°C	
Ni100	-80°C	+180°C	
Ni1000	-60°C	+150°C	

Resistance			
Input	Min	Max	
Low	0 Ohm	500 Ohm	
High	0 Ohm	2000 Ohm	

Potentiometer			
Input Min Max			
<500 Ohm	0 %	100 %	
<2000 Ohm	0 %	100 %	

Channels: 2

Input Type: RTD (Pt100, Pt1000, Ni100, Ni1000)

Resistance and Potentiometer (up to 2KOhm)

Calibration Accuracy:  $\pm 0.1$ °C for RTD;  $\pm 0.1$  Ohm for Resistance;

± 0.1 % for Potentiometer;

RTD Linearity: ± 0.2 °C

RTD Excitation Current: 0.350 mA typ.

Lead wire resistance influence: < 0.05 %/Ohm (50 Ohm max.) for 3 wires RTD

Thermal Drift: ± 0.005 % F.S. /°C for RTD

Sampling Rate: 10 samples/sec

Bandwidth: 4 Hz



### **DAT 6013 - DAT 6023**

Voltage		
Input	Min	Max
10 V	-10 V	+10 V

Current		
Input	Min	Max
20 mA	-20 mA	+20 mA

Channels: 2 ( DAT 6013 )

4 ( DAT 6023 )

Input Type:  $\pm$  10V or  $\pm$  20 mA \*

Calibration Accuracy:  $\pm 0.05 \%$ Linearity:  $\pm 0.1 \%$ 

Input Impedance: > 1MOhm for V; 47 Ohm for mA

Thermal Drift:  $\pm 0.005 \%$  F.S. /°C Sampling Rate:  $\pm 0.005 \%$  F.S. /°C

Bandwidth: 4 Hz

It must be to defined at order (V or mA).

### **DIGITAL INTERFACE**

Supply Voltage: 24 Vdc typical (30 Vdc max)

ON state voltage: > 9 Vdc

Input Impedance

(ENABLE, CLK): 4.7 KOhm

Minimum Output Load

(DATA): 560 Ohm

Maximum Clock signal frequency:

< 500 Hz (with 1ms filter)

< 50 Hz (with 10ms filter)

Debounce Filter: settable to 1ms or 10 ms

Rise Time: <0.2 ms

<sup>\*</sup> For DAT 6023 the input type is not configurable.



### SUPPLY

Supply Voltage: 18 to 30 Vdc Supply Current: 35 mA @ 24 Vdc

Polarity reversal protection: 60 Vdc

### **Temperature and Humidity**

Operating Temperature:  $-10 \div +60$  °C Storage Temperature:  $-40 \div +85$  °C Relative Humidity (not condensing):  $0 \div 90$  %

### **EMC**

Emission EN50081-2 Immunity EN50082-2

RF Immunity tested @ 10 V/m up to 1000 Mhz

### Housing

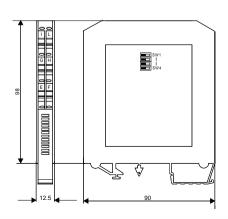
Material Selfestinguishing Plastic

Mounting DIN Rail Weight 50 g. approx.

Dimensions

(W x H x T) in mm: 90 X 98 X 12.5

# Mechanical Dimensions (mm)





### How to Program the module

The input type is in-field configurable by means of the dip-switches. The input type configuration is made by SW1..SW3 dip-switches which can be used to set up to 8 different input types. The standard correspondance between the dip-switch setting and the relative input type is shown in the tables below. It can be modified using the 'PRO6000' software and the PRODAT-03 interface.

By this way, it is possible to reconfigure the module for a wide range of input signal types at any time.

Also the CLK signal's digital filter can be set to 1 ms or 10 ms (half-period duration) by a dip-switch (SW4). The digital filter eliminates all the signal variations shorter than the specified time, avoiding undesired command simulations.

Hereafter the standard tables of the various modules are shown:

DAT6012 and DAT6013 modules, having a limited number of possible input types, are availables with a fixed table. Whereas DAT6011 and DAT6021 are available as in Tab.A or in Tab.B, indicating the choice at the order, or in any desired configuration using the software, as previously mentioned. DAT6023 module is not configurable; consequently the input type (V or mA) must be defined at the order phase.

DAT6011 - DAT 6021

SW1	SW2	SW3	Input	Input
			Tab.A	Tab.B
0	0	0	TcJ	50 mV
0	0	1	Tc K	100 mV
0	1	0	TcT	500 mV
0	1	1	Tc E	1000 mV
1	0	0	Tc R	
1	0	1	Tc S	
1	1	0	Tc B	
1	1	1	Tc N	

DAT6012

SW1	SW2	SW3	Input
0	0	0	Res. L
0	0	1	Res. H
0	1	0	Pt100
0	1	1	Ni100
1	0	0	Pt1000
1	0	1	Ni1000
1	1	0	Pot. L
1	1	1	Pot. H

### DAT6013

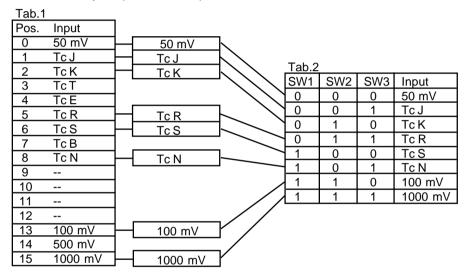
SW1	SW2	SW3	Input
Х	Х	0	10 V
Х	Х	1	20 mA



### How to create an Input Table

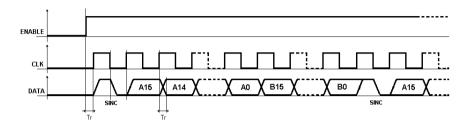
All the possible input types of the module are listed in a main table (Tab.1). It is possible to associate up to 8 of this input types to each one of the 8 dip-switch combinations, following the order of Tab.1 and compling to every choosed type the first free dip-switch combination. By this way the 'dip-switch to input type' correspondence table is created (Tab.2).

The example is referred to DAT6011 module and shows how to associate the height dip-switch combinations to three 'mV' inputs (50mV/100mV/1000mV) and five 'Tc' inputs (Tc J/K/R/S/N):



In any case, it is sufficient to set the desired data in the "PRO6000" program, and the table will be automatically created. Moreover the software will provide to program the module in the correct way.

### **Data Reading**



The data transfer is made sending an enabling signal (ENABLE) and a clock signal (CLK). If the ENABLE signal is high, a bit composing the reading is provided on the output (DATA) at every clock pulse.

Every reading cycle is composed of 1 synchronism bit followed of a 16 bit word for each analog input signal (channel). So that any reading is composed of 33 bits for 2-channels and 65 bits for 4-channels.

The synchronism bit indicates that the next bit is the most significant bit of the first channel value (A15); the following remaining bits of this value will be transmitted down to the least significant bit (A0). This bit will be followed by the most significant bit of the second channel value (B15), down to the least significant bit (B0). After the last bit, a new synchronism bit will be transmitted.

The value to be transmitted will be updated during the transmission of the synchronism bit. During the reading cycle, the ENABLE signal must stay at logic level HI.

The first bit after the ENABLE signal rise front will be a synchronism bit.

The synchronism bit level is high when the CLK signal is high and is low when the CLK signal is low. Differently, each data bit is updated on the CLK rise front and mantains its level until the next CLK rise front.

At any moment it is possible to send a rise front on the ENABLE signal to restart the reading cycle (by the synchronism bit).

The 'Debounce Filter' eliminates all the signal variations shorter than the specified time, avoiding undesired command simulations.

### **DATEXEL**

# PRELIMINARY DAT 6000

### How to write the PLC's instructions

The correct procedure to acquire the measures by the module can be described as following:

### Start condition:

ENABLE low and CLK low, then DATA is automatically low. Initialization:

- 1 ENABLE High
- 2 Wait for Tr

### Synchronism:

- 3 CLK High
- 4 Wait for Tr
- 5 Read DATA
- 6 DATA logic level must be 1 otherwise go to point 3 \*
- 7 CLK Low
- 8 Wait for Tr
- 9 Read DATA
- 10 DATA logic level must be 0 otherwise go to point 3 \*

### Bit reading:

- 11 CLK High
- 12 Wait for Tr
- 13 Read DATA
- 14 CLK Low
- 15 Wait for Tr
- 16 Read DATA
- 17 DATA logic level read on point 13 and on point 16 must be the same, otherwise go to point 3  $^{\star}$
- 18 Save the DATA logic level as bit in the reading register

### Channel reading:

- 19 Repeat points 11 to 18 for all the 16 bits of the measure, writing the bits in the reading register from the most significant one down to the least significant one
- 20 Repeat points 11 to 19 for all the channels to read
- 21 After the 16° bit of the last channel (2nd or 4th) return to point 3

To abort the reading without to read all the channels:

- 22 Be sure the CLK is Low
- 23 ENABLE Low
- 24 Wait for Tr
- 25 Go to point 1

NOTE: 'Tr' is the Debounce Filter time setting (1ms or 10 ms)

<sup>\*</sup> Synchronization is failed, then disregard the last reading. The data acquisition will be delayed until the next synchronism bit will be recognized. It is advisable to abort the reading procedure going to point 22.



The following two examples, each one toghether with its flow-graph, illustrate the procedure to be followed for writing the PLC's instructions.

### EXAMPLE n°1: 2 or 4 channels reading

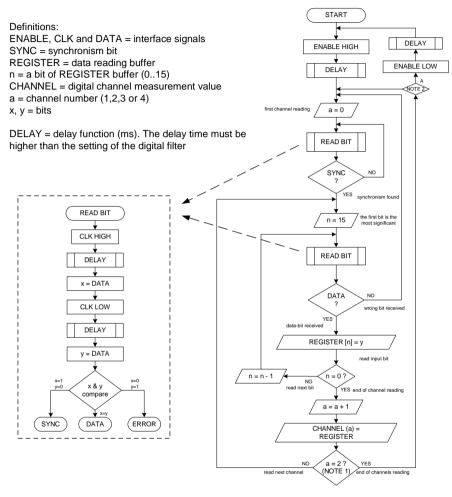
#### Definitions: ENABLE, CLK and DATA = interface signals SYNC = synchronism bit REGISTER = data reading buffer START n = a bit of REGISTER buffer (0..15) CHANNEL = digital channel measurement value DELAY ENABLE HIGH a = channel number (1,2,3 or 4) x. v = bitsDELAY ENABLE LOW DELAY = delay function (ms). The delay time must be NOTE 2: higher than the setting of the digital filter a = 0READ BIT The first hit is the most significant READ BIT READ BIT CLK HIGH REGISTER [n] = v DELAY read input bit CLK LOW n = n - 1 n = 0.7DELAY read next hit YES end of channel reading y = DATAa = a + 1CHANNAEL (a) = REGISTER YES a = 2.2(NOTE 1) read next channel end of channels reading

NOTE 1: to be modified following the number of channels to be read ( write " a = 4?" for the 4 channels reading) NOTE 2: follow the (A) option to reset the device or for not reading the unused channels

The procedure is fast and with few instructions because there are not synchronism controls. However, if the synchronism is lost (i.e. for a noise), the reading will be wrong. To avoid that, it is advisable to use the ENABLE signal to synchronize the procedure at the reading start.



### EXAMPLE n°2: 2 or 4 channels with synchronism control



NOTE 1: to be modified following the number of channels to be read ( write " a = 4 ? " for the 4 channels reading )

NOTE 2 : follow the (A) option to reset the device or for not reading the unused channels

The continuous control of the received bit allow a sure synchronization of the procedure. When the synchronism is lost, the next reading will be surely correct because it will starts only when a synchronism bit will be recognized. It is not necessary to use the ENABLE signal.

### **Data Format**

The module acquires the analog signal value of each channel and converts it in a digital string (bit). Each analog signal is converted in a 16 bit word which is serially transmitted as before described.

Then, it is possible to convert the received string in the corresponding decimal value, considering that each value is expressed in signed integer (the most significant bit indicates the sign: 0=positive 1=negative).

The user will must insert the decimal point as illustrated in the following tables.

Input	Decimals	Format
+/- 50 mV	3	+50.000
+/- 100 mV	2	+100.00
+/- 250 mV	2	+250.00
+/- 1000 mV	1	+1000.0
+/- 20 mA	3	+20.000
TcJ., TcN	1	+1200.0

Input	Decimals	Format	
RTD (°C)	1	+850.0	
Res (Ohm)	1	+2000.0	
Pot (%)	1	+100.0	

### Examples:

Input	Binary	Hex	Decimal	Measure
Ohm	0000 0000 0000 0001	0001	1	0.1 Ohm
100 mV	0010 0001 0011 0100	2134	8500	85.00 mV
1000 mV	1111 1111 1111 1111	FFFF	-1	-0.1 mV
TcJ	1111 1000 0011 0000	F830	-2000	-200.0 °C

## NOTE:

# DAT3023 4 Channel Voltage PLC Input

Phone: +1 561 779 5660 E-mail: Info@datexel.com - Web Site www.datexel.com